



Fermi National Accelerator Laboratory

CDF Run IIb

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Junction Port Card – Data and Control Board

--PRELIMINARY NOT FOR DISTRIBUTION--

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1 Introduction

This document describes the junction port card (JPC) for the upgrade of CDF (run IIb). The JPC is the interface between the FIB transition module IIb (FTMIIb) [1] and the mini port cards (MPC) [2]. Each JPC interfaces to five MPC and half FTM (Figure 1). The JPC is assembled in the cooling channels located on the face of COT, thus limiting the board's size. Due to the space limitations imposed by the assembly location, the JPC is divided in two different boards: data board and power supply board. The data board (JPCDB) is responsible for repeating the LVDS signals from and to the FTM, while the power supply board (JPCPS) regulates the voltages going to the MPC. This document describes the JPCDB only. For more information on the JPCPS refer to [3]. In total CDF RunIIb has 180 MPCs, 90 for each side of the detector. Hence there is a total of 18 JPC per side for the MPC and 8 JPC for the L0 hybrids, giving a total of 26 JPC per side, 52 total.



Figure 1 – Block diagram

2 JPC Data Board

The JPCDB is composed of connectors to the FTM interface, connectors to the MPC interface, and LVDS repeaters, as shown in Figure 2 and Figure 3. The 3M 100-mil pitch header connectors are used to interface with the FTMIIb, and the Omnetics connectors interface to the MPC. Since the space available in the JPCDB is not enough to fit a 68-pin header, this connector is split into two 100-mil pitch header connectors with 20 and 50 pins.

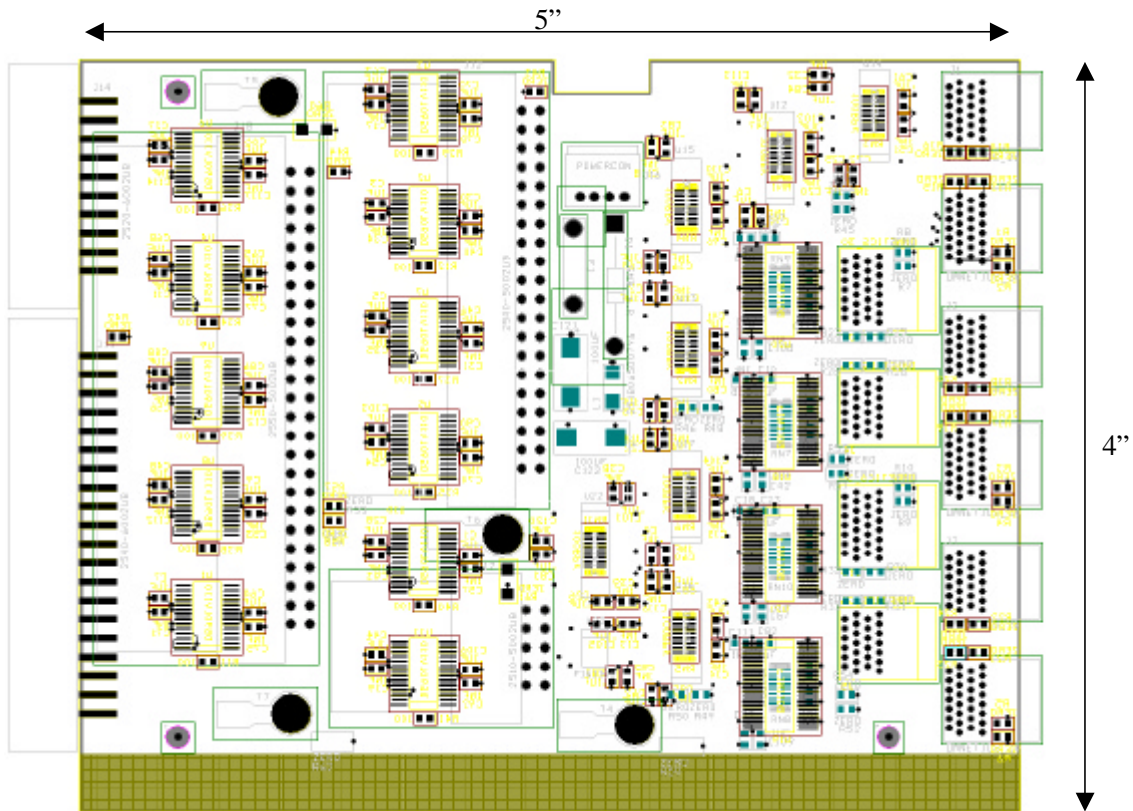


Figure 2 – JPC data board preliminary part placement, top view

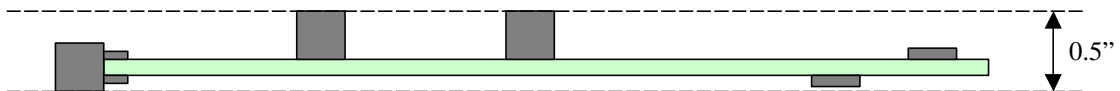


Figure 3 – JPC data board preliminary part placement, side view

Figure 4 shows a block diagram of the connections in the JPCDB.

2.1 Shield Connection

The 100-mil pitch header connectors on the JPC don't have a shield connection. For this reason the optional connection of the cable shield to the JPC digital ground is done via a connector ring (Figure 5). A 22AWG wire connects this terminal to the cable shield. The JPCDB has a thru hole pad to which the terminal may be screwed. This pad in the JPCDB is connected to a resistor to ground.

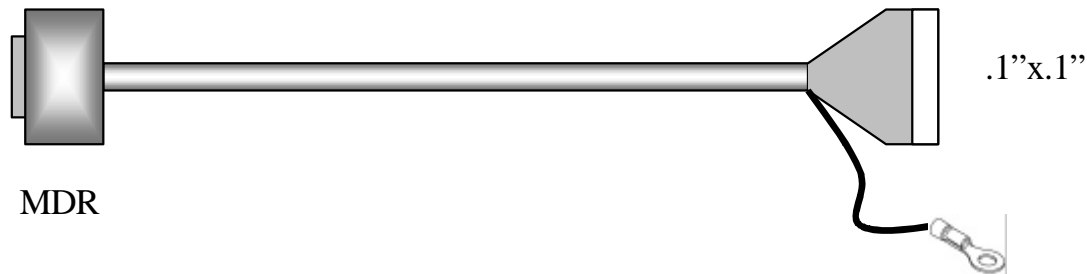


Figure 5 – Cable from FTM to JPC

2.2 Signal Fanout

The following signals are fanned out from the FTM to the JPC: PIN, BECLK, L1A, CLA_SR, BEMODE, FEMODE, CHMODE, PRD1, PRD2, CONTR, and PARST. Each of these signals is connected to two LVDS drivers in the JPC (Figure 6).

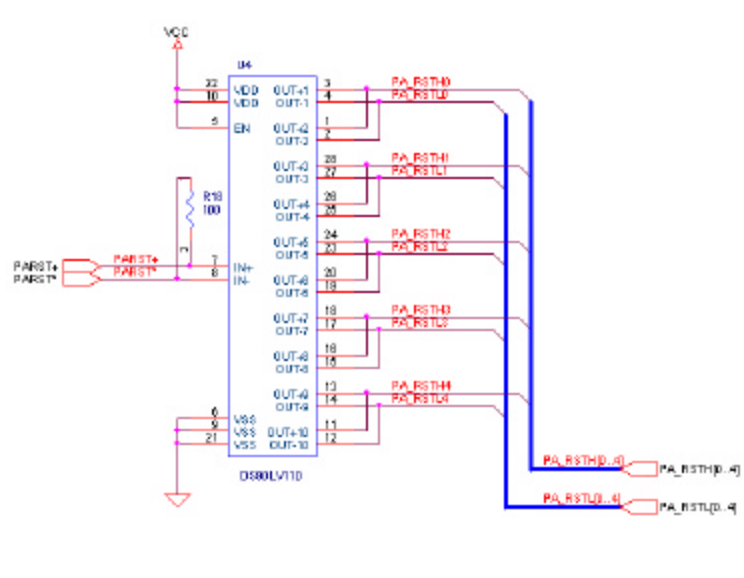
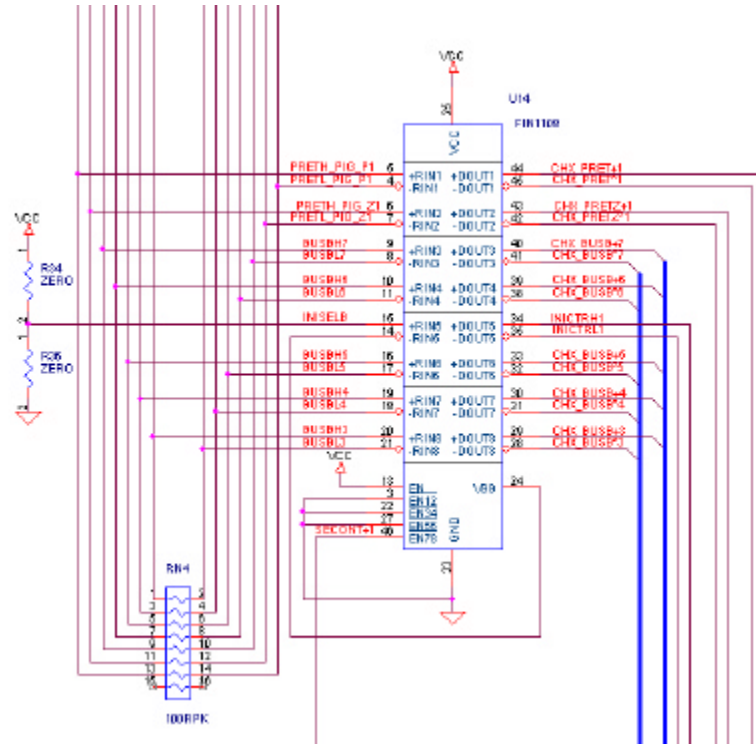


Figure 6 – JPCDB Fanout

2.3 Priority In

The PIN from the JPC to each stave can be initialized using PINP or PINZ (depending if the phi or z side is initialized first). The selection of initialization order is defined by the signal INITCTR (Figure 7). If INSEL is connected to VCC the

initialization is in normal operation mode (phi side first), and if INSEL is connected to GND the stave is configured in inverse operation mode (z side first).



2.4 Bi-directional LVDS Drivers

The SVX4 chip used in run IIB has three bi-directional LVDS lines: bus0, bus1, and bus3. These signals are used during readout as data lines, and during digitize as control lines. In order to accommodate the change of signal direction, the JPCDB has bi-directional drivers that are controlled by the same signal that controls the MPC drivers (SECONT). Hence the driving direction of the JPC and MPC drivers always agree.

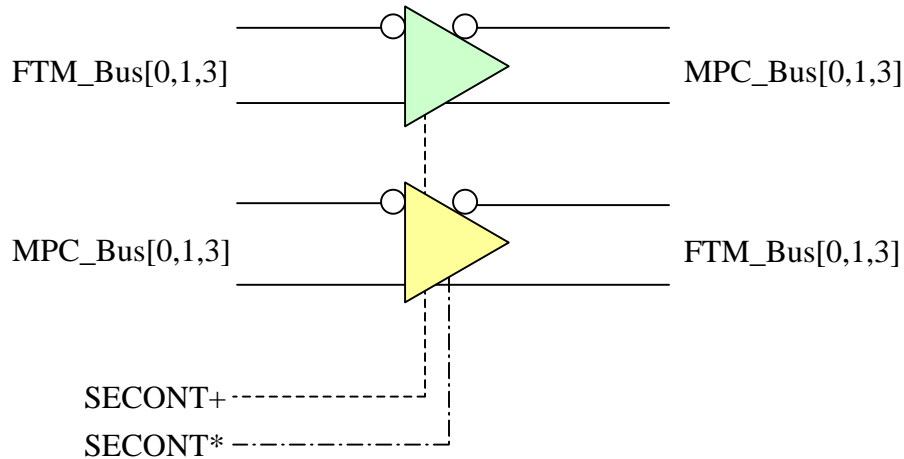


Figure 9 – Bi-directional LVDS drivers

2.5 Power Connector

The 3.3V power to the JPCDB is provided by the JPCPS. The power connector is a four pins Hirose connector (DF3A-4P-2DS). The voltage is regulated in the JPCPS, so the JPCDC has filtering, over current, and surge protection.

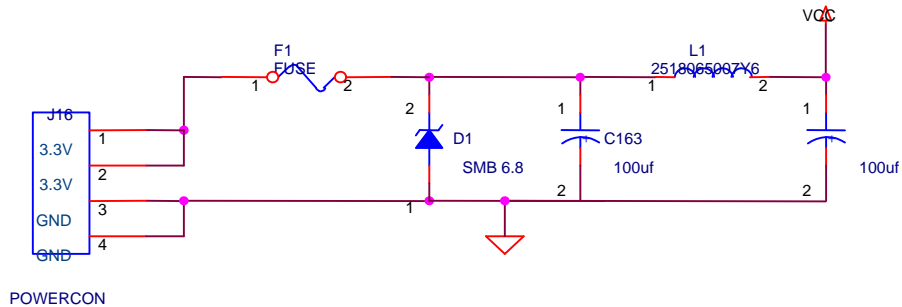


Figure 10 – Power supply interface

2.6 RTD Interface

Each stave has a RTD for temperature measurement. The RTD signals are available at the JPCDC in a 10 pins header connector.

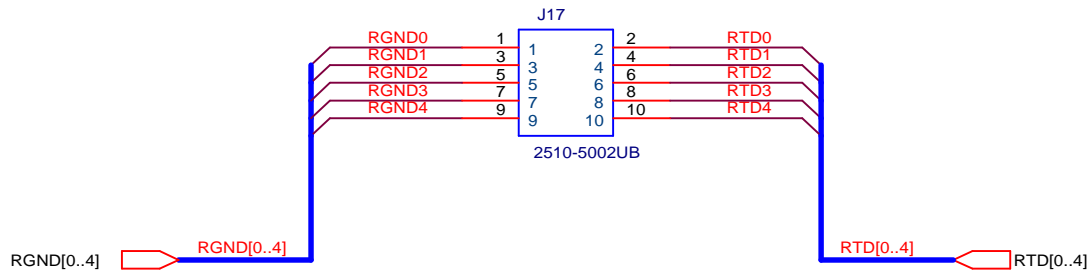


Figure 11 – RTD interface

3 Mechanical and Electrical Specifications

Each of the LVDS drivers in the JPCDC board dissipates a maximum of 0.4W (DS90LV110) and 0.25W (FIN1108). Since the board has 11 DS90LV110 drivers and 11 FIN1108 drivers, the estimated total power dissipation is approximately 7W. The drivers are in close thermal contact to the ground plane of the board, which is thermally connected to the COT cooling channel via the support bar.

The final dimensions of the JPC are yet to be defined. The pre-production card is 5" by 4", but the dimension of the production boards will be defined by inspecting the installation site (on the face of the COT, Figure 12) during the September 2003 shutdown.

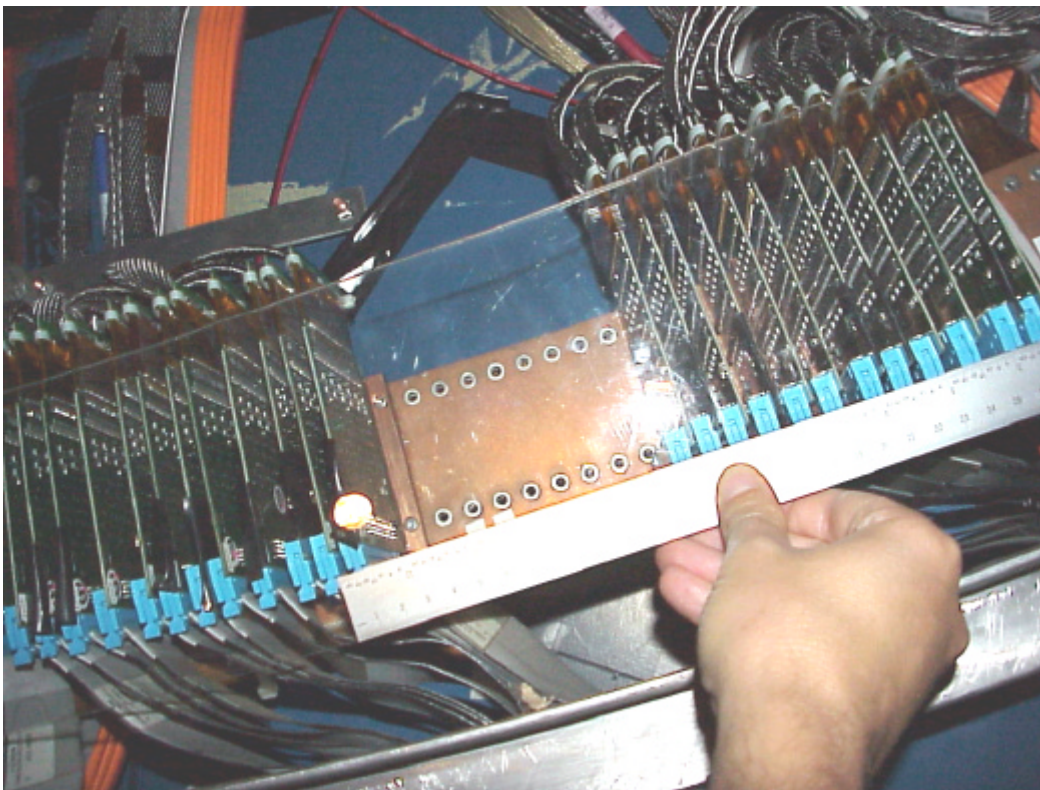


Figure 12 – Face of COT cooling channel

4 References

- [1] Andresen, A., Cardoso, G., Zimmermann, S., “FIB Transition Module IIb,” Fermilab internal document ESE062402, June 2002
- [2] Andresen, A., Cardoso, G., Zimmermann, S., “Mini Port Card,” Fermilab internal document ESE20011104, November 2001
- [3] Cardoso, G., Turqueti, M., “Junction Port Card – Power Supply Board,” in preparation.
- [4] Cardoso, G., et al. “Ten Bits Differential Transceiver (0.25 μ m),” Fermilab internal document ESE-SVX-020502, July 2002.